IN THE CLAIMS

Please cancel Claims 1-5, 18-23, 45, 46, 50, and 51 without prejudice or disclaimer.

Claims 1-5 (cancelled)

Claim 6 (currently amended): ~~The sampling circuit of claim 5,~~ A sampling circuit to sample a source signal received on an input path, a noise signal of high frequency components also being received on said input path, said sampling circuit comprising:

a first circuit portion receiving an input signal on said input path, said input signal containing both of said source signal and said noise signal, said first circuit portion generating an output signal by limiting bandwidth of said input signal, wherein said noise signal being substantially absent in said output signal due to said limiting; and

a second circuit portion sampling said output signal generated by said first circuit portion,

wherein said first circuit portion comprises a low pass filter,

wherein said second circuit portion is implemented as a switched capacitor circuit,

wherein said low pass filter comprises:

a resistor receiving said source signal on one terminal and other terminal of said resistor being connected to a first node; and

a first capacitor connected between said first node and a second node,

wherein said first circuit portion further comprises:

a first switch connected between said second node and a common mode voltage; and

a second switch connected across said first capacitor, and

wherein said second circuit portion comprises:

a buffer being coupled to receive an input from said first node;

a second capacitor connected between a third node and a fourth node;

a third switch connected between an output of said buffer and said third node; and

a fourth switch connected between said fourth node and said common mode voltage.

Claim 7 (original): The sampling circuit of claim 6, wherein said sampling circuit is implemented without requiring a bandwidth limiting element in signal path.

Claim 8 (currently amended): The sampling circuit of claim ~~1~~ 6, wherein said second circuit portion and said first circuit portion are implemented using a separate set of components.

Claim 9 (original): A sampling circuit to sample a source signal received on an input path, a noise signal of high frequency components also being received on said input path, said sampling circuit comprising:

a first circuit path sampling an input signal containing both of said source signal and said noise signal; and

a second circuit path sampling high frequency components of said input signal, wherein a difference of outputs of said first circuit path and said second circuit path is generated as a sampled output of said sampling circuit, said noise signal being substantially absent in said sampled output due to said difference.

Claim 10 (original): The sampling circuit of claim 9, wherein said first circuit path comprises a first switched capacitor circuit.

Claim 11 (original): The sampling circuit of claim 10, wherein said second circuit path comprises:

a high pass filter providing high frequency components in said input signal as a first output; and

a second switched capacitor circuit coupled to said high pass filter sampling said first output.

Claim 12 (original): The sampling circuit of claim 11, wherein said high pass filter comprises:

a first capacitor receiving said input signal on one terminal and a second terminal of said first capacitor being connected to a first node; and

a resistor connected between said first node and a second node.

Claim 13 (original): The sampling circuit of claim 12, wherein said second circuit path further comprises:

a first switch connected between said second node and a common mode voltage; and

a second switch connected across said first capacitor.

Claim 14 (original): The sampling circuit of claim 12, wherein said second switched capacitor circuit comprises:

a second capacitor connected between a third node and a fourth node;

a third switch connected between a fifth node and said third node; and

a fourth switch connected between said fourth node and said common mode voltage.

Claim 15 (original): The sampling circuit of claim 14, wherein said second circuit path further comprises a buffer connected between said first node and said fifth node.

Claim 16 (original): The sampling circuit of claim 15, wherein said sampling circuit is comprised in a correlated double sampler (CDS) which receives a reference level in a first phase and a relative video level in a second phase, said CDS generating actual video level representing a pixel as a difference of said reference level and said relative video level.

Claim 17 (original): The sampling circuit of claim 16, further comprising:

a third circuit path implemented similar to said second circuit path, wherein said first circuit path samples said reference level along with a corresponding noise signal in said first phase and said relative video level along with a corresponding noise signal in said second phase,

said second circuit path sampling high frequency components corresponding to said reference level in said first phase and said third circuit path sampling high frequency components corresponding to said relative video level in said second phase;

an amplifier amplifying the difference of outputs of said first circuit path received on a first input and said second circuit path received on a second input at the end of said second phase;

a third capacitor connected between a first output of said amplifier and said first input of said amplifier forming a first feedback path in said second phase;

a fourth capacitor connected between a second output of said amplifier and said second input of said amplifier forming a second feedback path in said second phase, wherein the difference of outputs provided between said first output and said second output represents said actual video level.

Claims 18-23 (cancelled).

Claim 24 (currently amended): ~~The device of claim 23,~~ A device comprising:

a sampling circuit to sample an input signal comprising a source signal and a noise signal of high frequency components, said sampling circuit comprising:

a first circuit portion receiving said input signal, said first circuit portion generating an output signal by limiting bandwidth of said input signal, wherein said noise signal being substantially absent in said output signal due to said limiting; and

a second circuit portion sampling said output signal generated by said first circuit portion,

wherein said device captures an image in a digital form, said device comprises:

an image sensor allowing a light corresponding to said image to be incident on said image sensor, wherein said image sensor generating an electrical signal proportionate to the intensity of incident light; and

an analog front end (AFE) processing said electrical signal, said AFE comprising said sampling circuit, said input signal being generated based on said electrical signal,

wherein said first circuit portion comprises a low pass filter,

wherein said second circuit portion is implemented as a switched capacitor circuit,

wherein said low pass filter comprises:

a resistor receiving said source signal on one terminal and other terminal of said resistor being connected to a first node; and

a first capacitor connected between said first node and a second node,

wherein said first circuit portion further comprises:

a first switch connected between said second node and a common mode voltage; and

a second switch connected across said first capacitor, and

wherein said second circuit portion comprises:

a buffer being coupled to receive an input from said first node;

a second capacitor connected between a third node and a fourth node;

a third switch connected between an output of said buffer and said third node; and

a fourth switch connected between said fourth node and said common mode voltage.

Claim 25 (original): The device of claim 24, wherein said sampling circuit is implemented without requiring a bandwidth limiting element in signal path.

Claim 26 (original): The device of claim 25, wherein said second circuit portion and said first circuit portion are implemented using a separate set of components.

Claim 27 (currently amended): The device of claim ~~19~~ 24, wherein said image sensor contains a plurality of pixels, wherein each of said plurality of pixels stores a charge proportionate to the intensity of incident light and said image sensor generating said input signal proportionate to said charge.

Claim 28 (currently amended): The device of claim ~~21~~ 24, wherein said AFE further comprises:

a programmable gain amplifier (PGA) amplifying an output of said sampling circuit to generate an amplified sampled signal; and

an analog to digital converter (ADC) converting said amplified sampled signal to digital values representing said image.

Claim 29 (original): The device of claim 28, said device further comprises:

a processor processing said digital values; and

a memory storing said digital values.

Claim 30 (original): The device of claim 29, wherein said image sensor comprises a charge coupled device (CCD).

Claim 31 (original): A device comprising:

a sampling circuit to sample an input signal containing a source signal and a noise signal of high frequency components, said sampling circuit comprising:

a first circuit path sampling said input signal; and

a second circuit path sampling high frequency components of said input signal, wherein a difference of outputs of said first circuit path and said second circuit path is generated as a sampled output of said sampling circuit, said noise signal being substantially absent in said sampled output due to said difference.

Claim 32 (original): The device of claim 30, wherein said device captures an image in a digital form, said device comprises:

an image sensor allowing a light corresponding to said image to be incident on said image sensor, wherein said image sensor generating an electrical signal proportionate to the intensity of incident light; and

an analog front end (AFE) processing said electrical signal, said AFE comprising said sampling circuit, said input signal being generated based on said electrical signal.

Claim 33 (original): The device of claim 32, wherein said first circuit path comprises a first switched capacitor circuit.

Claim 34 (original): The device of claim 33, wherein said second circuit path comprises:

a high pass filter providing high frequency components in said input signal as a first output; and

a second switched capacitor circuit coupled to said high pass filter sampling said first output.

Claim 35 (original): The device of claim 34, wherein said high pass filter comprises:

a first capacitor receiving said input signal on one terminal and a second terminal of said first capacitor being connected to a first node; and

a resistor connected between said first node and a second node.

Claim 36 (original): The device of claim 35, wherein said second circuit path further comprises:

a first switch connected between said second node and a common mode voltage; and

a second switch connected across said first capacitor.

Claim 37 (original): The device of claim 35, wherein said second switched capacitor circuit comprises:

a second capacitor connected between a third node and a fourth node;

a third switch connected between a fifth node and said third node; and

a fourth switch connected between said fourth node and said common mode voltage.

Claim 38 (original): The device of claim 37, wherein said second circuit path further comprises a buffer connected between said first node and said fifth node.

Claim 39 (original): The device of claim 31, wherein said image sensor contains a plurality of pixels, wherein each of said plurality of pixels stores a charge proportionate to the intensity of incident light and said image sensor generating said input signal proportionate to said charge.

Claim 40 (original): The device of claim 38, wherein said AFE further comprises:

a programmable gain amplifier (PGA) amplifying an output of said sampling circuit to generate an amplified sampled signal; and

an analog to digital converter (ADC) converting said amplified sampled signal to digital values representing said image.

Claim 41 (original): The device of claim 40, said device further comprises:

a processor processing said digital values; and

a memory storing said digital values.

Claim 42 (original): The device of claim 40, wherein said image sensor comprises a charge coupled device (CCD).

Claim 43 (original): The device of claim 42, wherein said sampling circuit is comprised in a correlated double sampler (CDS) which receives a reference level in a first phase and a relative video level in a second phase, said CDS generating actual video level representing a pixel as a difference of said reference level and said relative video level.

Claim 44 (original): The device of claim 43, further comprising:

a third circuit path implemented similar to said second circuit path, wherein said first circuit path samples said reference level along with a corresponding noise signal in said first phase and said relative video level along with a corresponding noise signal in said second phase,

said second circuit path sampling high frequency components corresponding to said reference level in said first phase and said third circuit path sampling high frequency components corresponding to said relative video level in said second phase;

an amplifier amplifying the difference of outputs of said first circuit path received on a first input and said second circuit path received on a second input at the end of said second phase;

a third capacitor connected between a first output of said amplifier and said first input of said amplifier forming a first feedback path in said second phase;

a fourth capacitor connected between a second output of said amplifier and said second input of said amplifier forming a second feedback path in said second phase, wherein the difference of outputs provided between said first output and said second output represents said actual video level.

Claims 45 and 46 (cancelled).

Claim 47 (original): A sampling circuit to sample a source signal received on an input path, a noise signal of high frequency components also being received on said input path, said sampling circuit comprising:

means for sampling an input signal generates a first output, wherein said input signal contains both of said source signal and said noise signal; and

means for sampling high frequency components of said input signal generates a second output, wherein a difference of said first output and said second output is generated as a sampled output, said noise signal being substantially absent in said sampled output due to said difference.

Claim 48 (original): The sampling circuit of claim 47, wherein said means for sampling an input signal passes said input signal through a first switched capacitor circuit.

Claim 49 (original): The sampling circuit of claim 48, wherein said means for sampling high frequency components is operable to:

pass said input signal through a high pass filter to provide high frequency components in said input signal as a third output; and

pass said third output through a second switched capacitor circuit to generate said second output.

Claims 50 and 51 (cancelled).

Claim 52 (original): A method of sampling a source signal received on an input path, a noise signal of high frequency components also being received on said input path, said method comprising:

sampling an input signal to generate a first output, wherein said input signal contains both of said source signal and said noise signal; and

sampling high frequency components of said input signal to generate a second output, wherein a difference of said first output and said second output is generated as

a sampled output, said noise signal being substantially absent in said sampled output due to said difference.

Claim 53 (original): The method of claim 52, wherein said sampling an input signal comprises passing said input signal through a first switched capacitor circuit.

Claim 54 (original): The method of claim 53, wherein said sampling high frequency components comprises:

passing said input signal through a high pass filter to provide high frequency components in said input signal as a third output; and

passing said third output through a second switched capacitor circuit to generate said second output.